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Reversible logic circuit for next-generation edge computing applications using IBM quantum system

Muhammad Zohaib [a], Seyed-Sajad Ahmadpour [b,*], Bahman Javadi [c], Mojtaba Noorallahzadeh [d], Nima Jafari Navimipour [e,f]

[a] Department of Biomedical Engineering, Faculty of Engineering and Natural Sciences, Istanbul Atlas University, Istanbul 34083, Türkiye
[b] Department of Computer Engineering, Faculty of Engineering and Natural Science, Istanbul Atlas University, Istanbul, Türkiye
[c] School of Computer, Data and Mathematical Sciences, Western Sydney University, NSW 2751, Australia
[d] Department of Computer Engineering, Dez.C., Islamic Azad University, Dezful, Iran
[e] Department of Computer Engineering, Faculty of Engineering and Natural Sciences, Kadir Has University, Istanbul, Türkiye
[f] Research Center of High Technologies and Innovative Engineering, Western Caspian University, Baku, Azerbaijan

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ABSTRACT

Edge computing reduces latency by processing data nearer to its origin, improving real-time decision-making under applications like smart cities and autonomous systems that demand quick reactions. However, conventional edge architectures suffer from significant issues such as power consumption, computation, and security. In order to overcome these limitations, this study combines the quantum-based reversible logic in edge computing by designing a reversible arithmetic and logic unit (ALU) implemented with IBM Quantum Laboratory. The proposed reversible ALU uses a Feynman gate (FG), a Reversible Multiplexer (RMUX1) gate, and an NMG6 gate to guarantee the logical reversibility and the preservation of information with the least dissipation of energy. The circuit is simulated and verified using the IBM Quantum laboratory. Its performance is evaluated using quantum cost (QC), garbage output (GO), constant input (CI) and number of gates (GC) metrics. In addition, simulation results together with a literature-based comparison indicate that the proposed reversible ALU achieves favorable QC, GO, CI, and GC metrics relative to selected earlier reversible ALU designs. These circuit-level results indicate the potential of reversible quantum design principles for low-power and efficient computation in future edge-oriented architectures. The presented circuit-level results indicate the potential of reversible quantum design principles for low-power computation in future edge-oriented architectures.

1. Introduction

The development of an intelligent society and rising human needs have led intelligence to permeate multiple industries as well as everyday life [1]. Every aspect of society today incorporates edge devices [2] through their presence in intelligent homes and self-driving vehicles, as well as security cameras and smart factory robots [1]. Moreover, Fig. 1 demonstrates the edge computation system with reversible quantum-based ALU processes for measuring data. Measurement information on incoming data is analyzed locally to give fast and efficient processing [3,4]. Low-energy, highly accurate computations in reversible quantum ALU make the measurement more accurate. The results are further refined by a feedback loop that guarantees both reliable and accurate outputs of the measurements. The Edge System utilizes quantum and reversible arithmetic logic units through its integration to achieve enhanced performance, together with better efficiency in intelligent applications. The implementation of edge computing deals with several significant challenges that stem from restricted processing capabilities, elevated power consumption, and security threats [3,4].

Edge devices produce increasingly large datasets that traditional computing systems have difficulty processing effectively. The main problem revolves around power usage because edge devices experience restricted energy capabilities in their operating environments [5]. Standard processors face time limitations because their calculations delay their ability to run advanced data processing tasks [6]. The combination of security and privacy threats degrades these challenges because distributed edge systems are easier targets for cyberattacks [7]. A new computational framework must be developed because it needs to

* Corresponding author.
E-mail address: seyed.ahmadpour@atlas.edu.tr (S.-S. Ahmadpour).

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Fig. 3. Reversible NOT gate used is a fundamental reversible logic element [25].

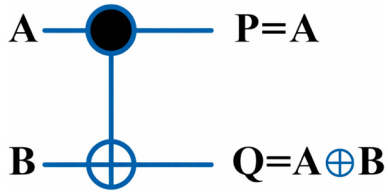

Fig. 4. Feynman gate structure, a reversible controlled NOT gate used for signal copying and inversion [26].

development of a reversible Arithmetic Logic Unit (ALU) through the IBM Quantum Laboratory. The ALU operates reversibly under IBM's quantum logic gate scheme while minimizing power loss and improving computational throughput, so it is a suitable solution to edge computing limitations [23].

This study investigates the combination of quantum computing frameworks with edge computing to develop enhanced computational architectures with improved efficiency and scalability.

The primary contributions of this research are as follows:

- Proposing a reversible ALU architecture design for edge computing using quantum principles.
- Designing and implementing a reversible ALU circuit in the IBM quantum laboratory to achieve energy-efficient computations.
- Analyzing the circuit-level efficiency of the proposed reversible ALU in the IBM Quantum Laboratory environment using QC, GO, CI, and GC metrics.

The structure of this paper consists of the following sections: Section 2 explains the reversible logic technology. Section 3 discusses the existing related research. Moreover, section 4 consists of the suggested quantum-based circuit design for edge computing. Furthermore, Section 5 consists of experimental results and a discussion of performance analysis of the proposed research, and the paper concludes with future research in Section 6.

2. Background

A circuit is reversible because every input vector matches exactly one output vector, while the input and output vector numbers stay constant. A Boolean function $f : \{0,1\}^n \rightarrow \{0,1\}^n$ is reversible if it establishes a one-to-one correspondence between input and output vectors. It receives a reversible classification because every input sequence finds a distinct output sequence [24]. This gate, also known as the controlled-NOT (CNOT) gate, with a 1×1 structure.

It is regarded as one of the principal reversible gates. Fig. 3 shows the NOT gate. The reversible NOT gate has a quantum cost (QC) equal to one (QC = 1) [25].

The Feynman Gate is a fundamental reversible logic gate with essential applications in quantum computing and reversible circuit design [26]. This gate also known as the CNOT/controlled NOT gate, which is a 2×2. Fig. 4 shows the Feynman gate. In Eqs (1) and (2), A and B represent the inputs, and the Feynman gate QC = 1 [26].

$$P = A \tag{1}$$

$$Q = A \oplus \mathrm{B} \tag{2}$$

Research in quantum edge computing (QEC) needs to use classical edge computing (CEC) as its foundation instead of operating independently [27]. Future progress in QEC can extract significant benefits by examining the current developments within Edge Intelligence (EI) [28]. The primary goal of EI is to handle complicated or precision-demanding processor-intensive challenges that surpass traditional control-based software programs by utilizing AI accelerator hardware for executing deep neural network (DNN) models on limited-edge systems [28]. Moreover, QEC uses emerging mobile quantum processing units (QPUs) [29] to address optimization tasks and enhance precision for problem solving. This section creates interaction links by comparing QPU integration hurdles to the history of AI energy-efficient accelerator development. Within edge computing publications, the term "AI" usually describes machine learning and deep learning techniques when used to reference the field [30].

The term tensor processing units (TPUs) [31] serves as an inclusive definition for a family of AI hardware accelerators specially designed for mobile devices because they efficiently execute DNN operational graphs compiled by vendors [32]. The quantum phenomena of entanglement and superposition give QPUs their powerful computing edges. The combination of properties within QPUs lets them solve complex problems, including integer factorization and discrete algorithms, at speeds superior to those of traditional computing device [33]. Furthermore, classical TPUs improve deep learning model performance on edge devices, whereas QPUs accelerate different kinds of tasks that classical programming cannot handle [31]. Mobile quantum processing units (MQPUs) [10] operate similarly to TPUs through support of light DNNs, although their purpose involves executing shallow quantum circuits on constrained edge devices for optimization tasks [34].

However, two primary research directions for future QEC constitute quantum on edge (QoE) and quantum for edge (QfE) [10]. The QoE research branch seeks to merge quantum components with modern edge architectures to give distributed programs the ability to transfer operations to QPUs, effectively reducing system delays along with backend traffic. QfE explores the application of quantum algorithm solutions, which perform better than conventional AI approaches to edge computing, especially optimization problems. The primary goal of QfE study is to overcome classical performance in practical edge computing applications, but classical solutions still have some foundational applications [10].

3. Related work

An important research direction involves with a reversible design of ALUs with optimized gate-level architectures. Such as, Norouzi, Heikalabad [35] proposed a reversible ALU using QCA nanotechnology and Fredkin and HNG gates as a fundamental building block. Their architecture facilitates 20 logical and arithmetic functions with significant reductions in the number of cells and delay and it has a single-layer structure without cell rotation required and therefore easier to manufacture. Similarly, Faraji and Rezai [36] had suggested the use of a multi-layer reversible ALU (RALU) using HNG and Fredkin gates to improving its performance. Their architecture exhibited gains of area, latency, and power dissipation that indicate advantages of multi-layer QCA designs in difficult circuit design.

Another important line of research focuses on minimize power usage and enhancing energy efficiency in reversible QCA based ALUs. A reversible logic-based ALU was designed by Navimipour, Ahmadpour [37] to implement Feynman and Fredkin gates together with a reversible full adder, and was aimed at low-power digital circuit uses. Their findings show that they produce tremendous power consumption at different levels of power as compared with conventional designs. Jun, Wei [38] proposed reversible digital signal processing (DSP) architecture based on QCA architecture in a similar context. The focus of their approach is on the efficient use of resources as well as lowering the power

Table 1
Comparative analysis of existing works.

Ref.	Category	Key Contribution	Strengths	Limitations	Identified Research Gap
[35]	Reversible ALU (QCA)	Single-layer reversible ALU using Fredkin & HNG gates (20 operations)	Reduced cell count and delay; no cell rotation improves manufacturability	Higher clock phases; limited scalability analysis	Lack of optimization for quantum cost
[36]	Multi-layer QCA ALU	Multi-layer reversible ALU with improved area and energy efficiency	Lower latency, reduced power dissipation, compact design	Increased structural complexity; fabrication challenges in multi-layer QCA	Limited focus on scalability and integration with emerging computing platforms
[37]	Low-power Reversible ALU	QCA-based ALU focusing on power reduction using reversible logic	Significant energy efficiency improvement	Limited performance comparison with advanced designs; lacks delay optimization	No comprehensive optimization across multiple metrics (delay, cost, scalability)
[38]	DSP-oriented Reversible ALU	Energy-efficient ALU for DSP applications using QCA	Efficient resource utilization; suitable for DSP systems	Focused mainly on DSP; lacks general-purpose optimization	Limited adaptability to broader computing frameworks such as edge systems
[39]	Optimized Reversible ALU	Coplanar QCA ALU using Modified Fredkin & HNG gates	Significant reduction in cell count, area, delay, and quantum cost	Design complexity; limited discussion on system-level applicability	Lack of integration with quantum platforms and edge computing environments
[27]	Edge Quantum Computing	EQC simulator for hybrid quantum-edge systems	Enables exploration without physical quantum hardware; scalable research platform	Simulation-only; no hardware-level implementation	Absence of efficient circuit-level designs for practical realization
[40]	Hybrid Quantum-Edge Architecture	Integration of quantum computing with edge networks	Improved computation and security; scalable applications	High-level architecture; lacks hardware design details	Need for optimized low-level circuits to support hybrid systems
[41]	Quantum + Blockchain Edge	Secure serverless edge computing using quantum and blockchain	Enhanced security and dynamic resource allocation	Conceptual model; lacks implementation and performance validation	Missing efficient hardware-level realization for practical deployment

consumption and supporting many arithmetic and logic operations, which help overcome the computational constraints in the DSP applications.

There have been more optimization efforts aimed at reducing the complexity of hardware and enhancing the general circuit efficiency. Aliabadian, Golsorkhtabaramiri [39] proposed an enhanced reversible ALU design using Modified Fredkin gates and an HNG-based reversible full adder made of coplanar gates. Their adoption showed great enhancements in the key performance measures of the decrease in QCA cost, occupied area, cell count, and latency and a decrease in quantum cost. The obtained results indicate the beneficial impact of optimized gate configurations and coplanar design methods on the improvement of QCA circuit performance.

One of the current research trends in the field of study is the creation of frameworks and simulation platforms to assess hybrid quantum-edge systems. Indicatively, Passian, Buchs [27] suggested an Edge Quantum Computing (EQC) simulator that would facilitate the exploration and optimization of future architecture of edge computing with the assistance of quantum technologies. Their work points to the drawbacks of traditional cloud-based systems regarding dealing with large data volumes with high-performance, accuracy, and power efficiency requirements. Focusing on simulation-based assessment, the study presents the real-world concerns of the cost and complexity of physical quantum systems, thus permitting the scalable investigation of the emerging field.

A different line of work is concerned with the topic of hybrid architectures, which combine the capabilities of quantum computing with edge infrastructure. In these respects, Ma and Ding [40] have proposed a hybrid quantum-edge computing architecture, which provides the benefits of quantum computing and edge computing in terms of low-latency computing networks. Their model shows development in both computing power and security of the system, and also provides a scaling and efficient deployment of the application. It has also been demonstrated in the study that such hybrid architectures can provide better performance than standalone classical or quantum-based applications in certain cases, and therefore the underlying hardware should be efficient to enable these architectures.

Besides architectural and performance, there are security and resource management that are also investigated within the context of quantum-enhanced edge computing. A conceptual model, which combines quantum computing and blockchain technology with serverless edge computing environment, was recommended by Gill [41]. This strategy uses the serverless computing to dynamically assign resources to the IoT applications and edge computing to minimize the response latency. Blockchain integration improves the level of security in the system, and quantum computing is used to make the process speedier. This multi-technology integration highlights the possibility of integrating superior paradigms to tackle major challenges in the distributed computing systems.

Although these are being made, the majority of available literature is concerned with system level design, simulation frameworks, and high level architectural integration. Very little effort has been focused on the creation of effective, low-level circuit designs which can be directly synthesized to support such hybrid quantum-edge environments. Specifically, it has not been sufficiently studied how optimized and reversible logic circuits can facilitate energy-efficient and scalable edge computing systems. This limitation also indicates the necessity of designing high-performance reversible logic-based ALUs, including the offered work, to fill-in the gap between theory and the hardware implementation.

The capabilities of the current ALU designs Table 1 such as high quantum cost and limited scalability and the lack of support of new computing paradigms such as edge-quantum systems demonstrate the necessity of more efficient architectures. In that regard, reversible quantum-computing-based ALU designs have become a viable option, as they are capable of operating at low power, simplified computational complexity, and better flexibility to upcoming computing environments of the next generation.

4. Framework for quantum-based edge computing

The edge system handles service automation, cluster scaling, performance monitoring, and resource optimization, and keeps a precise track of system execution patterns [42]. The edge computing system enables real-time workload management through its resource schedule optimization, which provides smart capacity control between computing resources such as CPUs, GPUs, MQPUs, and QPUs [10]. Users execute classical and quantum applications through this system platform using runtime control with a metadata-driven programming interface [10]. This integrated system establishes foundational elements to create next-generation computing capabilities with enhanced speed, low power consumption, low occupied area, and high efficiency.

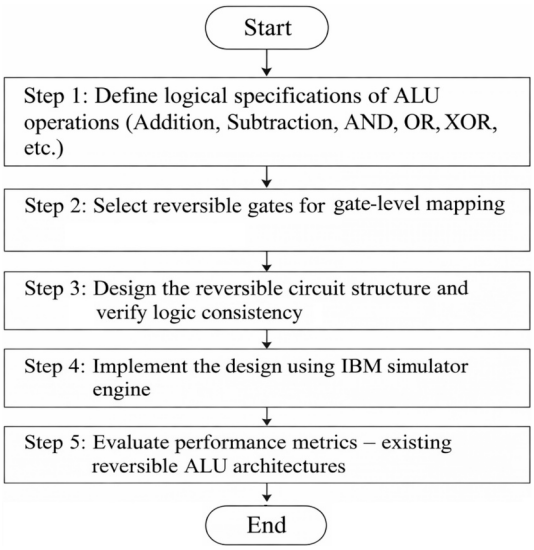

Fig. 5. Step-by-step methodology for implementing and evaluating the proposed reversible ALU using the IBM simulator.

4.1. Methodology and procedure of the proposed work

The proposed reversible ALU is systematically developed and evaluated through a sequence of well-defined stages, as summarized in the flowchart. The overall goal is to realize a logically reversible, energy-aware ALU and validate its functionality and performance on the IBM quantum laboratory.

Step 1. Definition of ALU specifications

First, the functional requirements of the ALU are specified. This includes identifying the set of arithmetic and logic operations (e.g., addition, subtraction, AND, OR, XOR, etc.), the word length, input/output formats, control signals, and any constraints on reversibility, fan-out, and ancilla usage.

Step 2. Selection of a reversible gate library

A suitable reversible gate library is chosen to implement these functions. In this work, the Feynman gate (FG) [23], Reversible multiplexer (RMUX1) [43] gate and NMG6 gate [44] are adopted due to their universality, low quantum cost, and compatibility with existing reversible/quantum synthesis strategies. Each ALU operation is mapped conceptually onto compositions of these gates.

Step 3. Reversible circuit design and logical verification

Based on the defined specifications and selected gates, the reversible circuit structure of the ALU is designed. Gate-level schematics are derived, ensuring one-to-one input–output mapping, no information loss, and minimal garbage outputs. Functional correctness is first validated at the logic level (truth-table and behavioural verification).

Step 4. Implementation on the IBM simulator

The validated reversible design is then encoded as quantum circuits using the IBM Quantum Laboratory. Qubits, quantum gates, and measurement operations are assigned according to the reversible ALU architecture, and the corresponding quantum code is generated.

Step 5. Evaluation of performance metrics (QC, GO, GC, CI)

Next, key reversible/quantum design metrics are computed:

- **Quantum Cost:** total cost based on the decomposition of multi-controlled gates into elementary quantum operations;
- **Garbage Outputs:** number of additional outputs required to preserve reversibility;
- **Gate Count:** Number of reversible/quantum gates used.

In addition, constant inputs in reversible logic are additional input lines fixed to 0 or 1 to enable reversible implementation of a desired function. Together, these metrics provide a quantitative assessment of the circuit-level efficiency and hardware cost of the proposed ALU.

Step 6. Comparative analysis with existing ALUs

Finally, the obtained metrics and functional behaviour are systematically compared with previously published reversible ALU designs. The comparison highlights the QC, GO, CI, and GC characteristics of the proposed design relative to selected earlier ALUs, thereby demonstrating its circuit-level efficiency. A step-by-step methodology for implementing and evaluating the proposed reversible ALU using the IBM simulator engine is illustrated in Fig. 5.

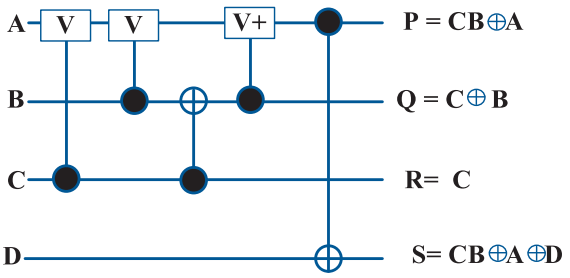

Fig. 6. Quantum realization of the NMG6 reversible block (NCV-level representation) [44] illustrating its structure and role as a fundamental logic primitive within the proposed ALU.

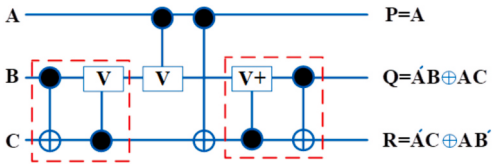

Fig. 7. Quantum representation of the RMUX1 (reversible multiplexer) block (NCV-level representation) [43], illustrating control-dependent reversible output selection in the proposed ALU.

4.2. Proposed reversible circuit for edge computing

4.2.1. Design motivation

Conventional edge-computing systems are constrained by power consumption and processing latency [45]. One source of this limitation is the irreversible nature of conventional complementary metal–oxide–semiconductor (CMOS) [46], in which lost information during computation. According to Landauer's principle, the irreversible erasure of one bit of information dissipates at least amount of energy as shown in Eq. (3) [47]. Reversible computation addresses this issue by enforcing a one-to-one mapping between input and output vectors, thereby avoiding information loss at the logic level. For this reason, reversible and quantum-compatible circuit design is a suitable approach for low-power edge-processing architecture.

$$E = KT\ln 2 \tag{3}$$

4.2.2. Reversible gate set

The proposed ALU is constructed using three reversible building blocks: the FG [23], the reversible multiplexer (RMUX1) [43], and the NMG6 gate [44]. The FG is employed for signal copying and XOR generation under the no-fan-out constraint of reversible logic. The RMUX1 gate is used for reversible routing and output selection according to the control inputs. The NMG6 gate is used in the function-generation stage to produce intermediate arithmetic and logic signals in a compact reversible form. The quantum-level realizations of the NMG6 and RMUX1 gates are illustrated in Fig. 6 and Fig. 7, respectively.

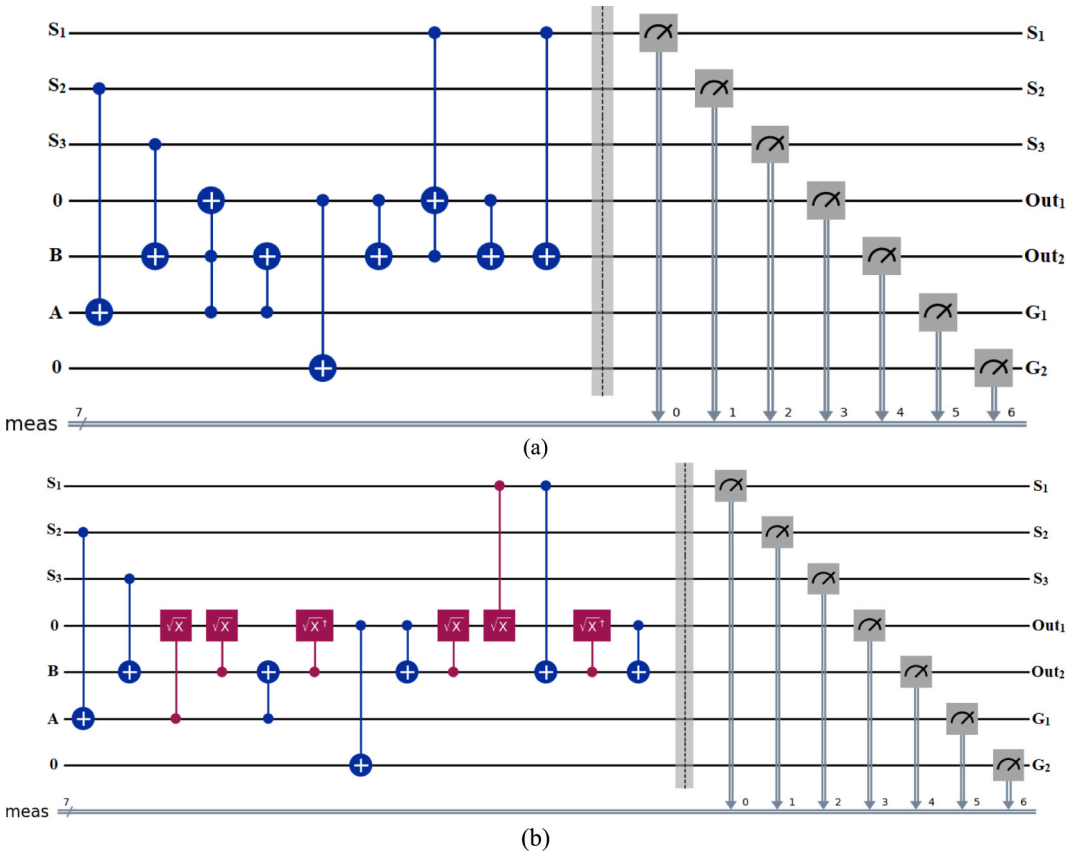

Fig. 8. Proposed reversible ALU showing (a) Toffoli-class and (b) NCV-level quantum decompositions of the design.

Table 2
Comparative analysis of quantum computing with edge computing.

Aspect	Edge Computing	Quantum Computing
Applications	– Real-time applications – IoT devices- Autonomous vehicles	– Cryptography – Optimization problems- Drug discovery
Advantages	– Low latency – Bandwidth conservation- Local data processing	– Massive parallelism – Solving complex problems- Enhanced data security
Challenges	– Management complexity – Limited computational resources- Synchronization issues	– Error correction – Quantum DE coherence- Limited availability of qubits
Integration	– Offloads processing from the cloud – Complements real-time analytics- Extends cloud capabilities to the edge	– Could enhance encryption at the edge – Could optimize cloud algorithms- May enable faster AI model training

4.2.3. ALU architecture and operation selection

As shown in Fig. 8, the proposed ALU accepts two operands, (A and B), one ancillary input initialized to logic 0, and three control signals, (S1, S2, S3). These control signals determine the required arithmetic or logic operation. Depending on the selected control pattern, the input operands are either directly processed or conditionally transformed before entering the reversible function-generation stage. The generated intermediate signals are then forwarded to a reversible selection stage, which routes the required result to the output without violating reversibility constraints. Through this structure, the same datapath supports both arithmetic operations, such as addition and subtraction, and logic operations, such as XOR, AND, and OR gates.

4.2.4. Toffoli-class representation and NCV decomposition

The proposed ALU is described using two complementary representations Fig. 8(a). Fig. 8(b) presents the corresponding NCV decomposition using the gate set $\{NOT, CNOT, V, V\dagger\}$, where v denotes the square-root-of-NOT gate and V† denotes its adjoint. This decomposition enables implementation within a standard quantum-gate library compatible with IBM Quantum Laboratory. In both representations, measurements are applied to the output qubits to obtain the classical output bits corresponding to the selected ALU operation.

Furthermore, Table 2 illustrates that integrated systems of quantum computing deliver substantial benefits to edge systems, as shown in a comparative analysis.

Table 2 provides a high-level conceptual comparison between edge computing and quantum computing. It is included to motivate the broader context of the work; however, the present study focuses only on the reversible ALU building block and does not implement the full integrated edge–quantum system

5. Simulation results

In this section, the findings are discussed that were obtained from quantum-level simulations carried out with IBM Quantum Laboratory, a popular framework built by IBM. The histogram in Fig. 9 reports the measurement outcomes (counts) obtained after executing the proposed reversible ALU on an IBM quantum laboratory. Therefore, Fig. 9 provides an empirical verification that the mapped Toffoli-class/NCV ALU circuit yields the intended output with a high probability. To illustrate the ALU input–output behavior under different configurations, representative examples of 7-qubit patterns are summarized below (bit ordering is reported consistently with the measurement register used in the implementation):

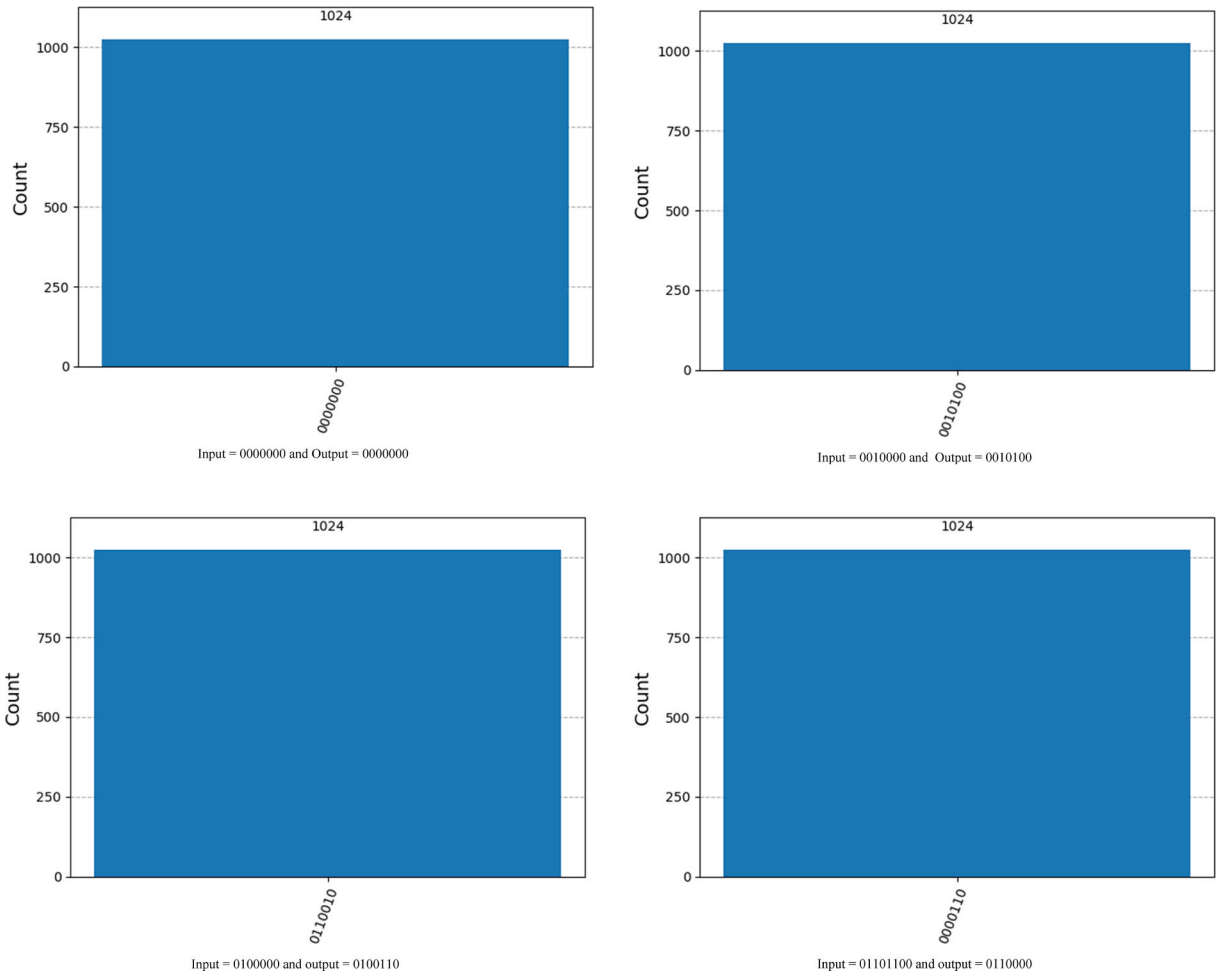

Fig. 9. Measurement histograms obtained from IBM Quantum Laboratory for representative input patterns of the proposed reversible ALU. The dominant output counts confirm the expected input–output mapping of the implemented circuit.

- Input: 0000000 → Output: 0000000
- Input: 0010000 → Output: 0010100
- Input: 0100000 → Output: 0100110
- Input: 0110110 → Output: 0110000

As shown in Fig. 9, each tested configuration produces a single dominant measurement outcome with a high count value, indicating that the implemented circuit preserves the intended reversible input–output relationship for the representative cases. This behavior provides practical validation of the correctness of the mapped ALU on the IBM Quantum Laboratory platform. Additionally, Table 3 illustrates the literature-based comparison of the proposed ALU with selected earlier reversible ALU designs, and Fig. 10 depicts the graphical representation of the quantum-based ALU circuit. The progress of quantum computing relies on circuits that are both efficient and can grow as needed, functioning within the boundaries of quantum hardware. The compared designs were reported under different technologies, gate libraries, and implementation assumptions; therefore, the comparison is indicative rather than a strict normalized benchmark.

Table 3 provides a literature-based comparison between the proposed ALU and selected earlier reversible ALU designs in terms of QC, GO, CI, and GC. The proposed design shows competitive circuit-level metrics relative to the selected references. Because the compared studies were developed under different technologies and assumptions, these comparisons should be interpreted as indicative rather than as a strict normalized benchmark. For Ref. [50], GC was not explicitly reported in the original source and is therefore marked as N/A. The corresponding average saving values were calculated using the available comparable metrics only.

Moreover, reducing the quantum cost leads to a smaller gate count, a shallower overall circuit, and faster execution, which can help reduce errors in quantum devices. This also improves quantum resource utilization and supports the effectiveness of the adopted circuit-optimization strategy. In addition, IBM Quantum Laboratory provides a practical platform for validating the hardware compatibility of the proposed design. Overall, the proposed design offers an efficient and low-overhead quantum logic structure and demonstrates promising feasibility for future quantum-oriented computing systems.

While this work does not claim a full security proof or a complete side-channel evaluation, the reversible ALU's information-preserving mapping is expected to reduce data-dependent switching signatures compared to irreversible designs, which can lower susceptibility to power/EM-based profiling. In future work, we will quantify this by collecting power/EM traces under controlled input patterns and reporting standard leakage metrics (e.g., correlation/DPA-style distinguishers), together with circuit-depth/noise sensitivity analysis after mapping.

6. Conclusion and future work

Edge computing enables low-latency data processing close to data sources. However, its scalability is constrained by limited processing capability, high energy consumption, and security concerns. Quantum computing and reversible logic provide a promising direction for

Table 3
Comparative analysis of quantum-based ALU with earlier designs.

Designs	Operations	QC	GO	CI	GC	Average Saving
[48] Design#01	6	19	3	2	8	
Improvement %	50	42.11	33.33	0	50	31.36
[48] Design#02	11	22	4	2	9	
Improvement %	8.33	50	50	0	55.56	38.89
[49] Design#01	6	21	2	2	6	
Improvement %	50	47.62	0	0	33.33	20.24
[49] Design#02	8	33	4	2	8	
Improvement %	33.33	66.67	50	0	50	41.67
[49] Design#03	12	25	5	4	6	
Improvement %	0	56.00	60	50	33.33	49.83
[50] Design#01	8	52	8	5	NA	
Improvement %	33.33	78.85	75	60	-	71.28
[50] Design#02	8	46	7	5	NA	
Improvement %	33.33	76.09	71.43	60	-	69.17
Proposed	12	11	2	2	4	

addressing some of these challenges at the circuit level by reducing information loss and improving energy efficiency. In this work, a reversible ALU was designed and functionally validated in IBM Quantum Laboratory. The results indicate promising circuit-level efficiency for future edge-oriented architectures, although this study does not claim a full edge-system implementation or a formal security proof. Compared with the best previously reported results, the proposed ALU achieves a 42.11% improvement in QC, while matching the best prior values for GO and CI. Future research will build upon the current findings through the following directions:

- Designing quantum gate optimization frameworks, which possibly can be run using machine learning algorithms, to minimize quantum cost, garbage, and circuit depth without compromising on high fidelity to the variety of quantum hardware backends.
- Integrating reversible logic unit with classical CMOS edge processors to create hybrid systems of quantum-edge computing that can dynamically switch between classical and quantum computation mode to achieve the best performance and power efficiency.
- Exploring quantum thermodynamic phenomena of reversible circuits to measure energy losses, transfer of entropy and information loss at the qubit level. Though the theoretical frameworks indicate that zero-energy loss of unitary operations is true, experimental studies in the future should confirm this principle in actual hardware.
- Extending the reversible ALU as a network computational node, which is modular and can be extended to quantum-edge networks, using entanglement-based communication and decentralized intelligence across autonomous systems.

CRediT authorship contribution statement

Muhammad Zohaib: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Seyed-Sajad Ahmadpour:** Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Investigation, Data curation, Conceptualization. **Bahman Javadi:** Writing – review & editing, Writing – original draft, Visualization, Supervision, Data curation, Conceptualization. **Mojtaba Noorallahzadeh:** Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Formal analysis, Data curation, Conceptualization. **Nima Jafari Navimipour:** Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization.

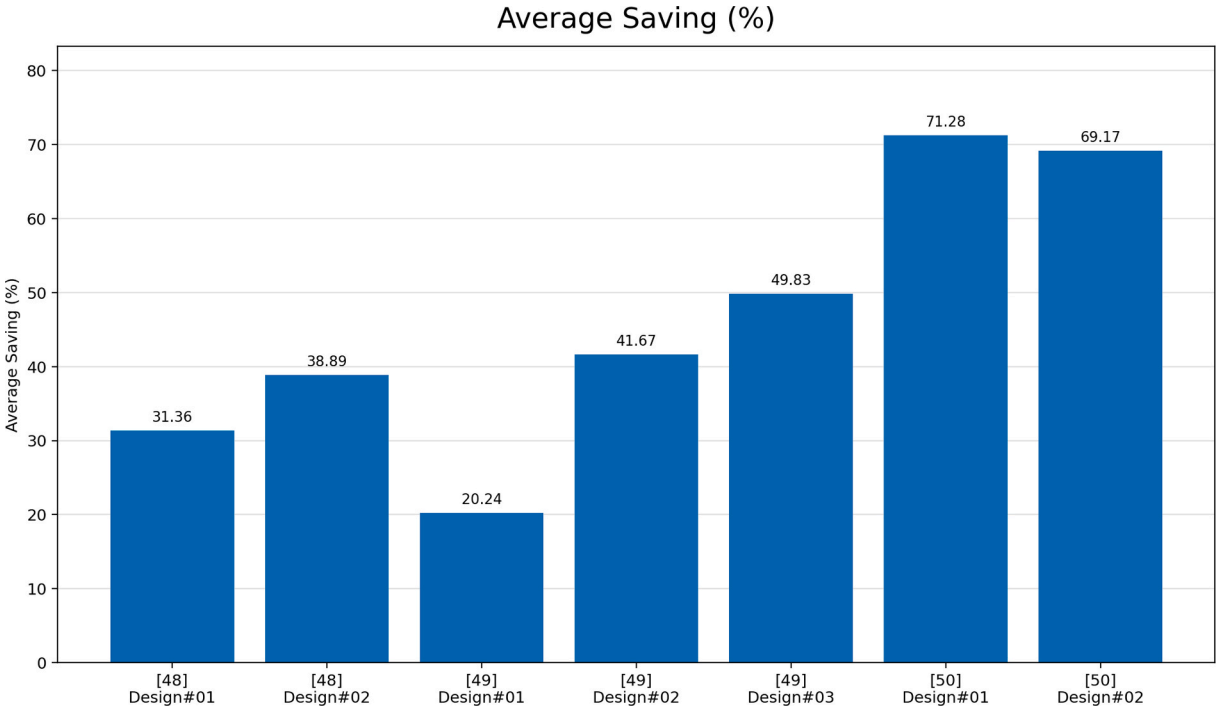

Fig. 10. Average Saving (%) of the proposed ALU relative to selected reference designs based on QC, GO, CI, and GC.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

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